EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 4

2/21/24 - 2/27/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

This week, we finished running through the analog design flow with an example inverter by simulating parasitic capacitances and began integrating with the Caravel Harness wrapper. However, due to LVS errors, the inverter has not been completely hardened and integrated. We were also able to narrow down the desired parameters of the ADC and have confirmed several architectures to be tested.

Past Week Accomplishments:

- Began inverter integration with Caravel Harness wrapper
- Began formulating prototyping plans for ADC architectures are ADC subsystems

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Gained a better understanding of how ReRAM operates and began inverter integration with the Caravel Harness	6	28
Gage Moorman	Passed DRC for inverter but ran into hiccup doing LVS. Decided on ADC design and timeline	6	28
Nathan Cook	Started looking at digital design flow and digital logic for ReRAM cells	6	27
Jason Xie	Began inverter integration with Caravel Harness Researched possible ADC architectures	8	28

Pending Issues:

- When integrating the inverter with the Caravel Harness, there are a couple of pins that trigger LVS errors
- Lack of data regarding process parameters for analog design

Plans for the coming week:

- Gage Moorman
    - Begin ADC design process with comparator design
    - Begin prototyping ADC design and figuring out best implementation
    - Find process parameters for analog design online or obtain them from simulations
- Konnor Kivimagi
    - Try to simulate a basic ReRAM cell in xschem to verify that the files are imported correctly.
    - Iron out any final kinks in the analog tool flow
    - Start prototyping an ADC design with the analog tools
- Nathan Cook
    - Start on making ReRAM cell in digital domain, testing for functionality by next week
    - Read up more on what needs to happen in the analog domain for the ReRAM to work
        - Possibly work on designs and voltage levels
- Jason Xie
    - Debug inverter integration LVS errors
    - Continue assisting in prototyping and testing suggested ADC designs
    - Begin looking into digital representation of ReRam Crossbar

Summary of Advisor Meeting:

During the advisor meeting, we presented and discussed ADC architectures and reviewed how ReRAM works. We also addressed how much area we have access to. Unfortunately, our meeting was cut short and that was all we could cover.